WHAT IS CLAIMED IS:

1. A flip chip type semiconductor device having pad and fuse areas, comprising:

an interlayer insulation layer formed on a semiconductor substrate;

a passivation layer formed on said interlayer insulation layer;

at least one first metal line formed in a given region of said passivation layer in said pad area;

at least a pair of second metal lines formed in a given region of said passivation layer in said fuse area;

a pad covering a portion of said first metal line;

a fuse covering said pair of second metal lines and said passivation layer therebetween, said fuse being formed of a layer of the same material as said pad;

a polyimide layer covering the whole surface of said semiconductor substrate including said pad and said fuse, said polyimide layer having a pad opening that exposes said pad; and

an under-bump metal layer pattern and a bump sequentially stacked on said exposed pad.

2. The device according to claim 1, wherein said passivation layer includes a lower silicon nitride layer, an intermediate silicon oxide layer, and an upper silicon nitride layer, which are stacked in order.

3. The device according to claim 1, wherein said first and second metal lines include a copper layer pattern and a diffusion barrier metal layer pattern enclosing side walls and bottoms of said copper layer pattern.

4. The device according to claim 3, wherein said diffusion barrier metal layer pattern is a tantalum nitride layer.

5. The device according to claim 1, wherein said pad and fuse include a barrier metal layer pattern and an aluminum layer pattern which are stacked in order.

6. A method of fabricating a flip chip type semiconductor device having pad and fuse areas, comprising the steps of:

forming an interlayer insulation layer on a semiconductor substrate;

forming a passivation layer on said interlayer insulation layer;

forming at least one first metal line and at least a pair of second metal lines in given regions of said passivation layer in said pad and fuse areas, respectively;

forming a metal layer over the surface of said semiconductor including said first and second metal lines;

forming a pad covering a portion of said first metal line and a fuse covering said pair of second metal lines and said passivation layer

therebetween, by patterning said metal layer;

forming a polyimide layer having a pad opening exposing said pad over the whole surface of said semiconductor substrate including said pad and said fuse; and

forming an under-bump metal layer pattern and a bump in order on said exposed pad.

7. The method according to claim 6, wherein said passivation layer is formed by depositing a lower silicon nitride layer, an intermediate silicon oxide layer, and an upper silicon nitride layer in order.

8. The method according to claim 6, wherein said step of forming said first and second metal lines includes:

forming at least one first groove and at least a pair of second grooves in said pad and fuse areas respectively, by patterning said passivation layer;

sequentially forming a conformal diffusion barrier metal layer and a copper layer filling said first and second grooves, over the surface of said substrate including said first and second grooves; and

planarizing said copper layer and said conformal diffusion barrier metal layer until a top surface of said passivation layer is exposed.

9. The method according to claim 6, wherein said metal layer is formed by depositing a barrier metal layer and an aluminum layer in

order.